



The two MSBbits of address are not decoded, so the following locations are identical:  
 I/O and RAM 0x--- = 0x4--- = 0xB--- = 0xC---  
 U29 / U28 0x2--- = 0x6--- = 0xA--- = 0xE---  
 U27 / U26 0x3--- = 0x7--- = 0xB--- = 0xF---

RAM must be populated in pairs:  
 0x0800-0x0BFF U18 (low nibble) with U20 (high nibble)  
 0x0C00-0x0FFF U19 (low nibble) with U21 (high nibble)

Component IDs begin at bottom left corner (nearest finger 1) and continue L to R  
 Row 1: U1 (74LS240) to U6 (74LS04)  
 Row 2: U7 (74LS244) to U12 (74LS175)  
 Row 3: U12 (MC6800) to U17 (74LS500)  
 Row 4: U18 (2114) to U24 (74LS32)  
 Row 5: U25 (74LS42) to U29 (2716)

Header J1 is on the right end of row 2, adjacent to U12  
 Header J2 is in row 4 between U23 (74LS42) and U24 (74LS32)